

### **ABSTRACT OF THE DISCLOSURE**

One embodiment of the present invention prioritizes resource utilization in a multi-thread processor. A priority register stores thread information for P threads. The thread information includes P priority codes corresponding to the P threads, at least one of the P threads requesting use of at least one resource unit. A priority selector generates assignment signal to assign the at least one resource unit to the at least one of the P threads according to the P priority codes.

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